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# MS-7673

ATX(Full Size)  
Ver: 20

## CPU:

INTEL - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH

## OnBoard Chipset:

ASM1083 PCIE to PCI Bri.  
HD Audio Codec:RTL892  
LAN:RTL 8111E 10/100/1000 NIC X 2  
SIO:FIN71889AD(LAA)  
FRONT USB3.0: UPD720200F1  
REAR USB3.0: UPD720200F1  
Flash ROM: 64 Mb SPI (PCH)  
1394 Controller: VT6315N

## Main Memory:

DDRIII (1066/1333MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 2  
PCI Express (X1) Slot \* 4  
PCI Slot \* 2(From ASM1083)

## PWM:

CPU:UPI6234(5PHASE)  
CPU\_VTT:UP6103A(1PHASE)  
CPU\_SA:UP6103A (1PHASE)  
DDR/PCH PWR:UP6103A

## Other:

SATA3.0 x2+SATA2.0 x4 (PCH)  
USB3.0 x4 (Rear\*2 Front\*2)  
USB2.0 \*4 (Rear\*8 Front\*4)  
COM Header \*1

## ACPI:

UPI

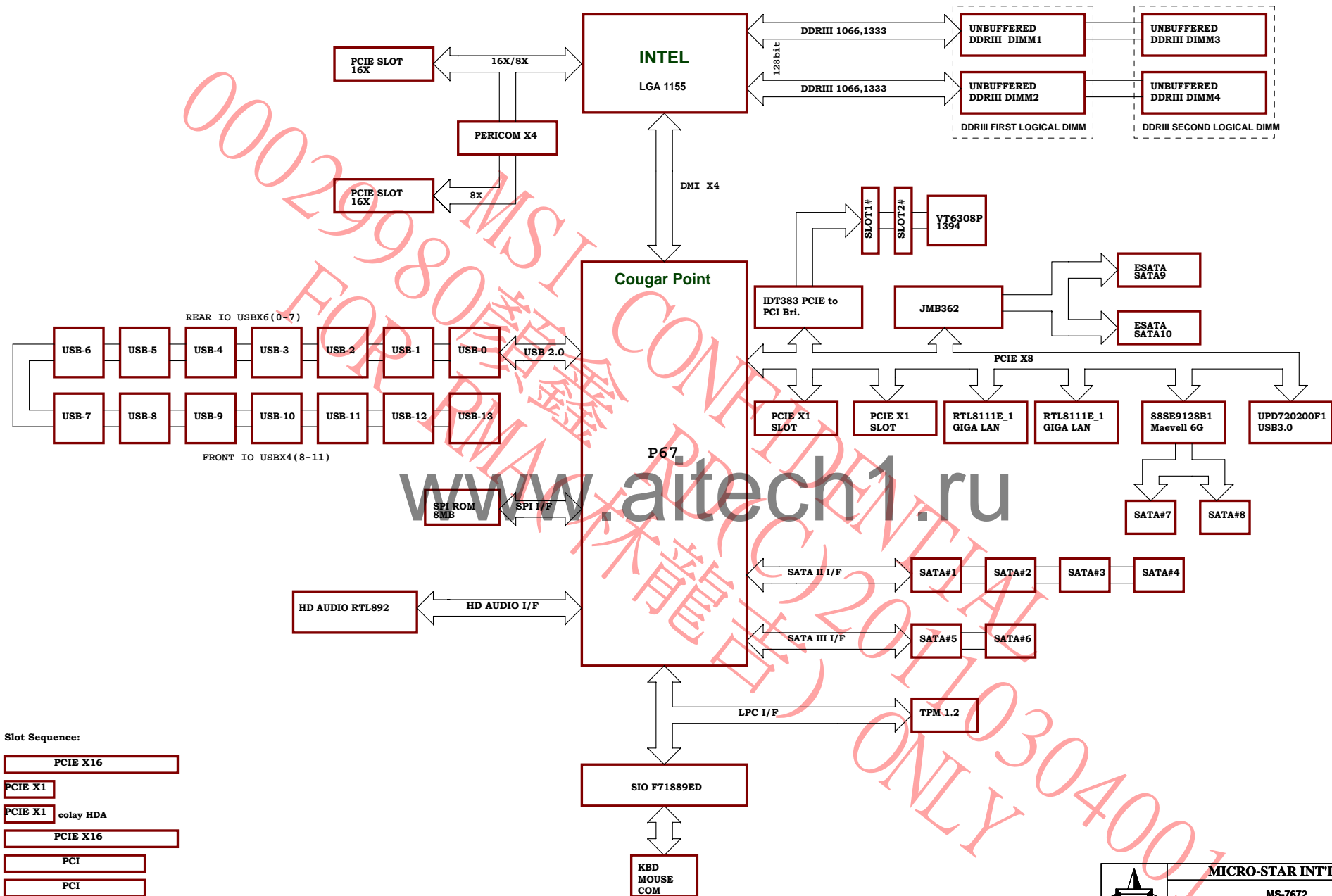


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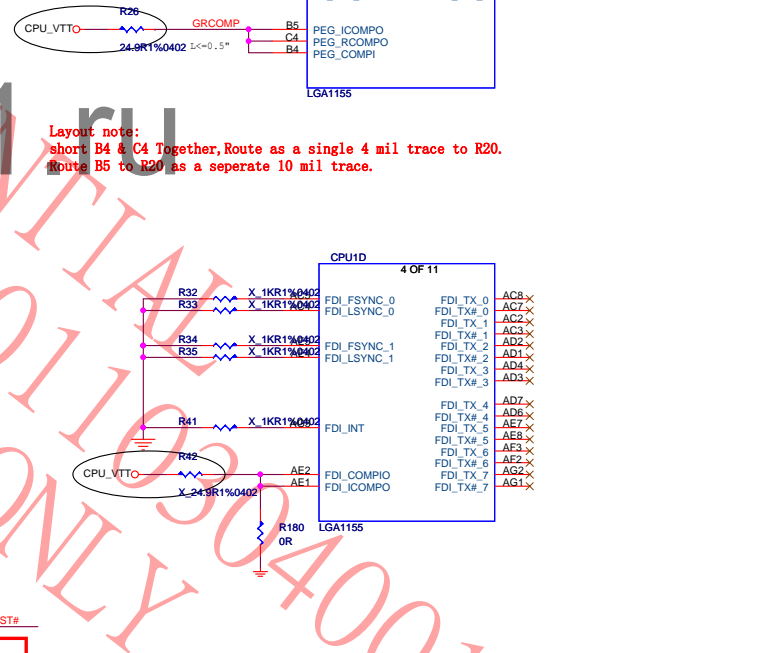
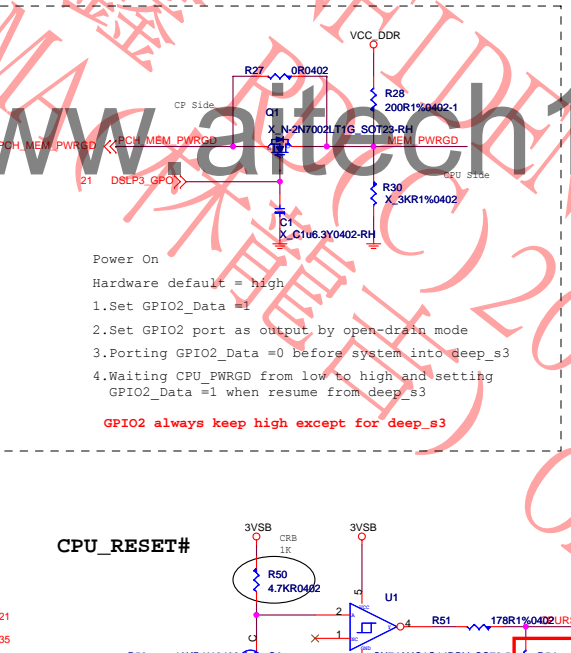
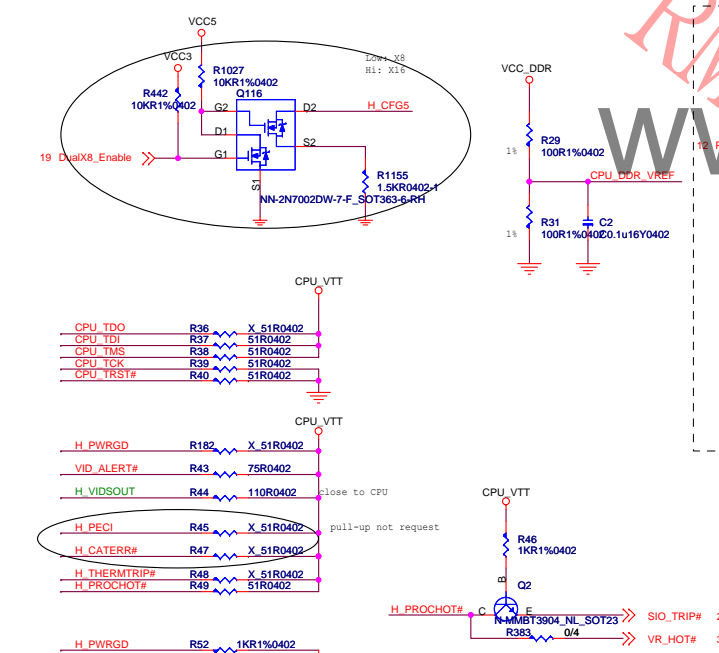
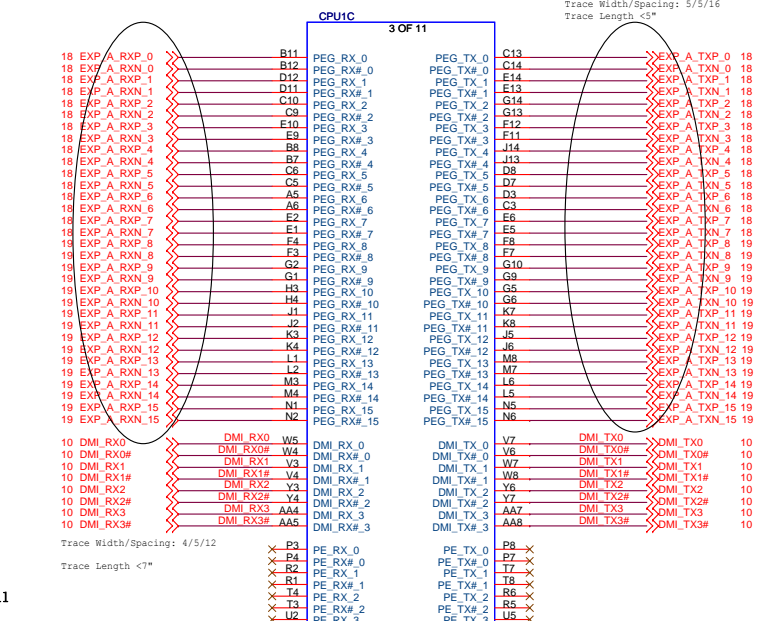
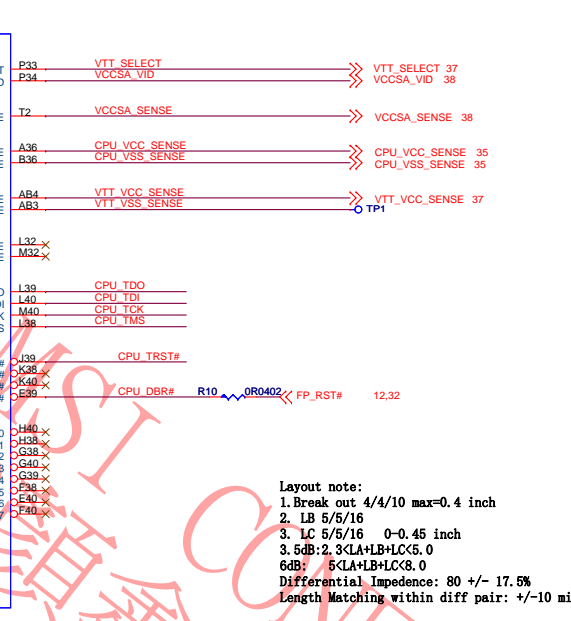
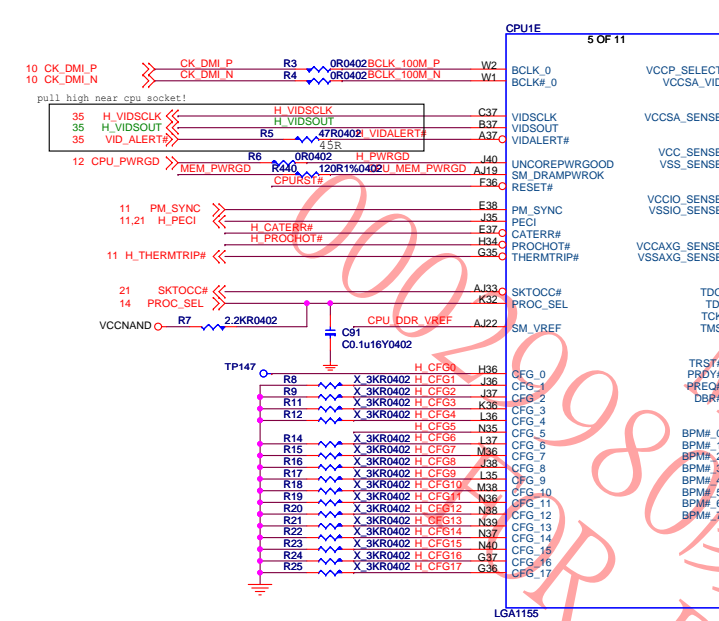
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PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8



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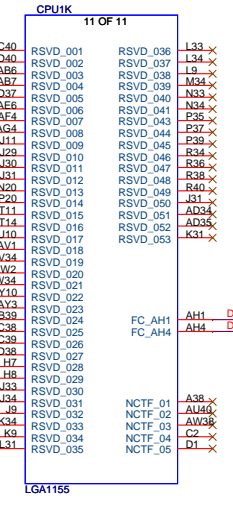
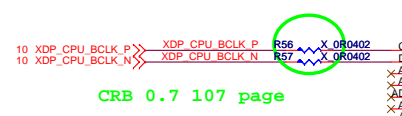
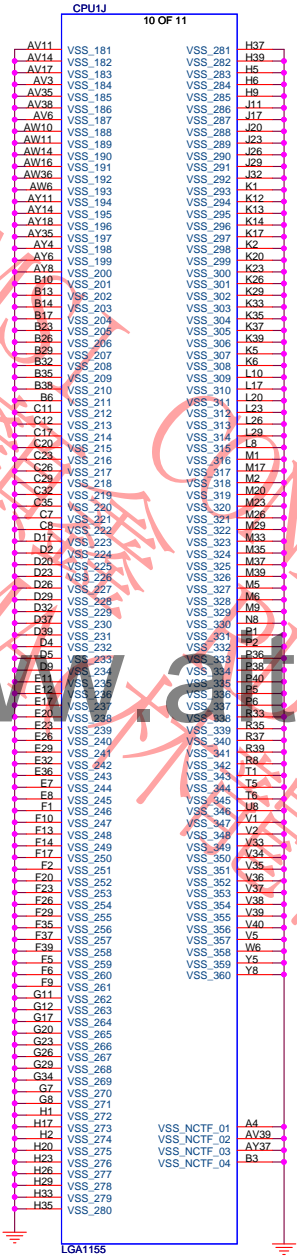
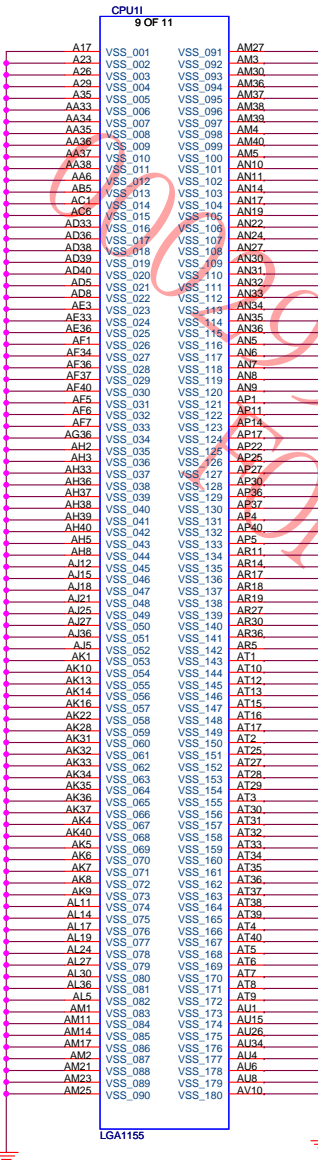












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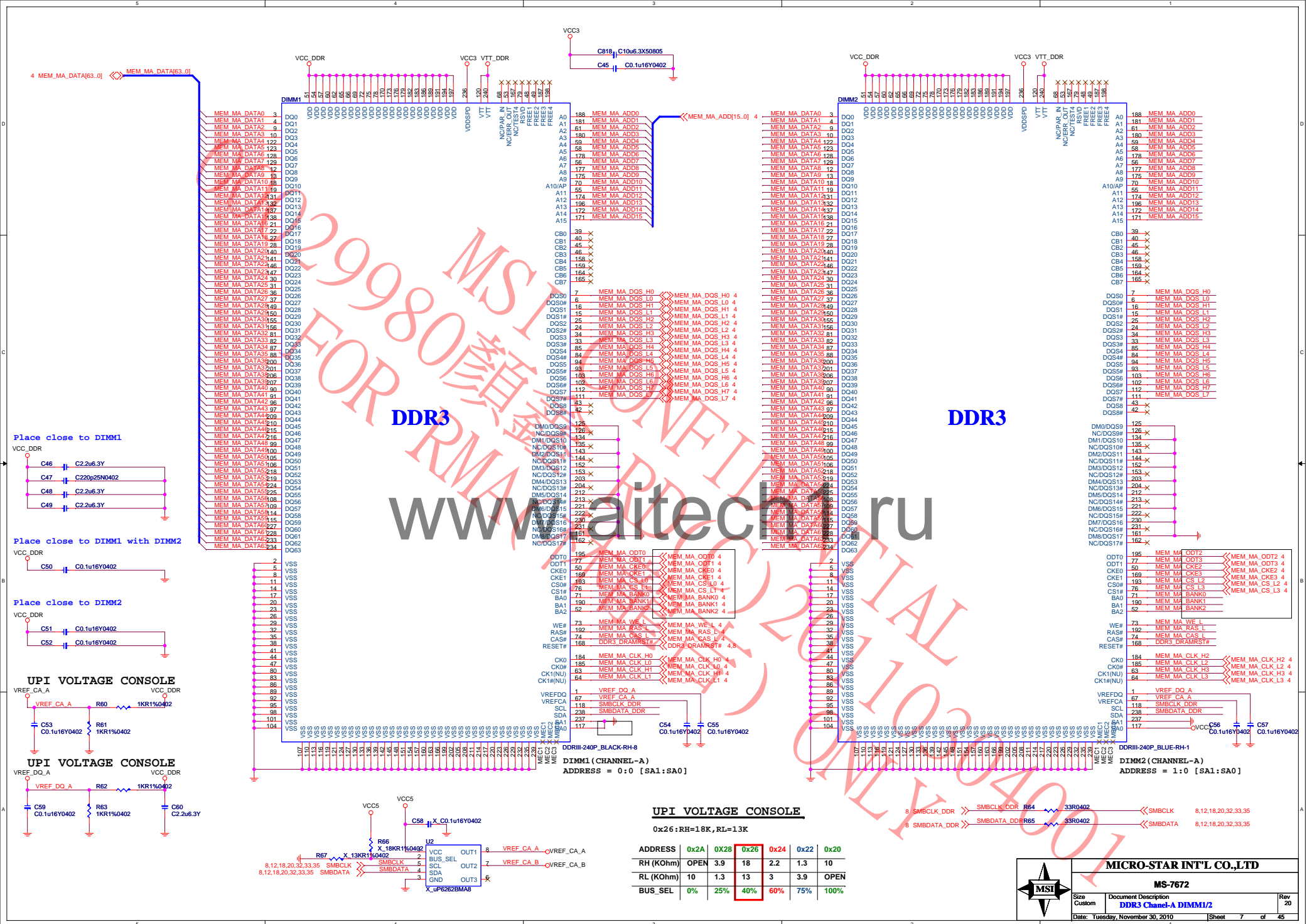


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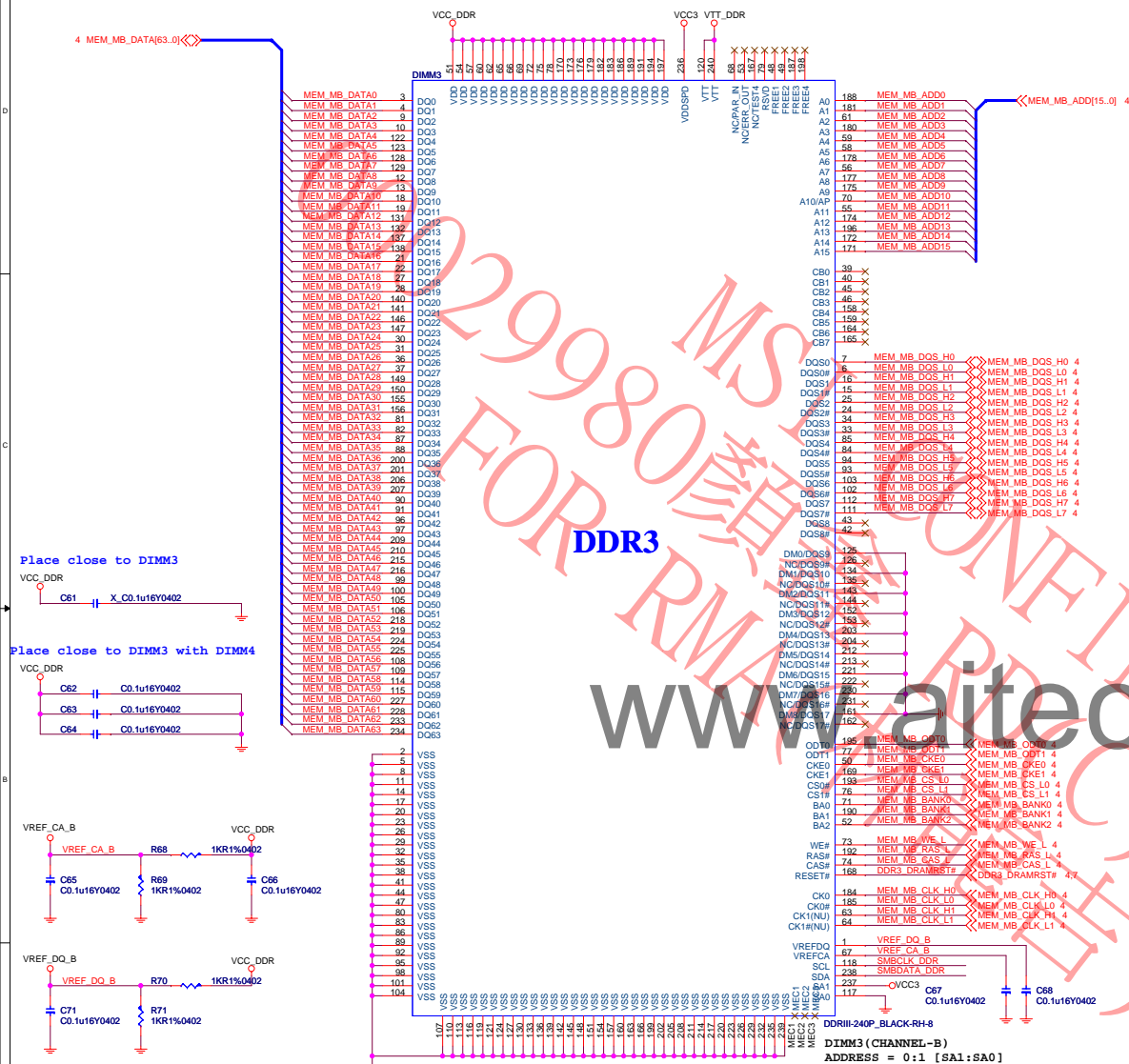
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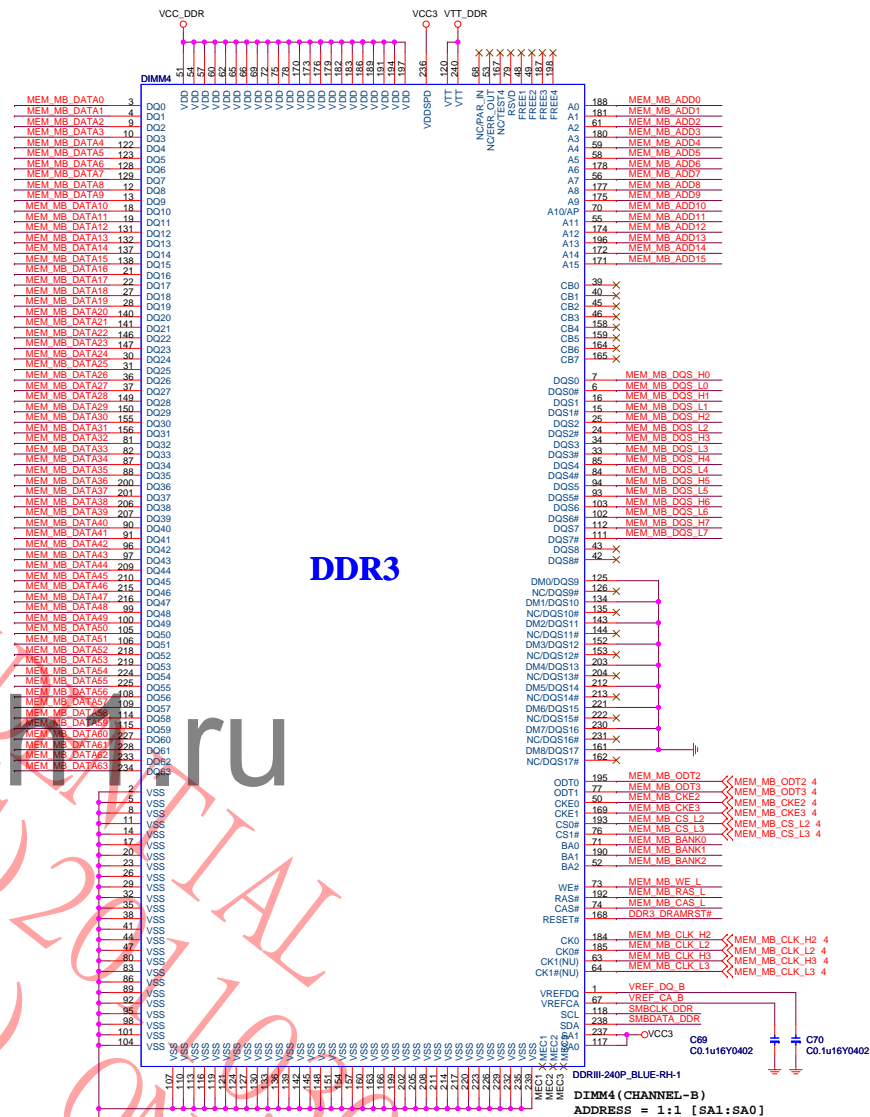




## DDRIII DIMM\_B0



## DDRIII DIMM\_B1



## UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=31

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	9.1	3	2.2	1.3	10
RL (KOhm)	10	3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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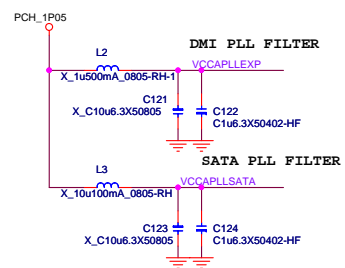




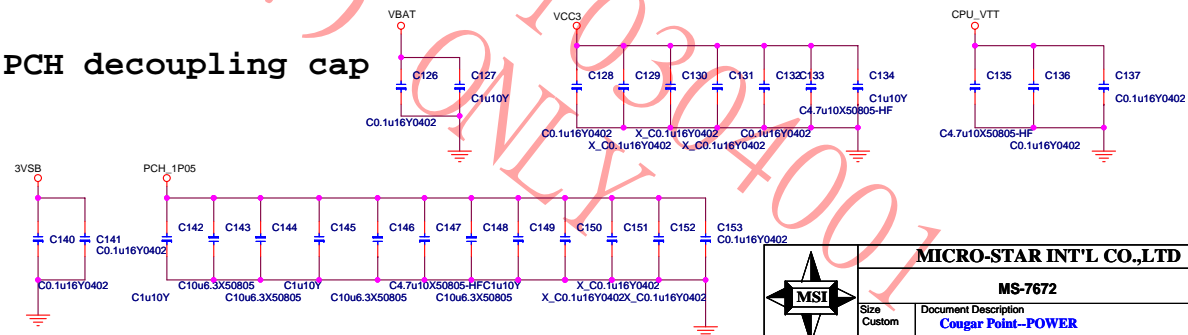
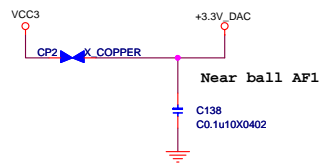
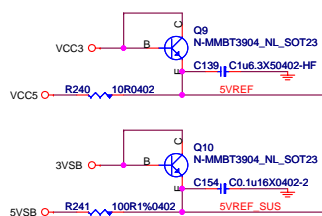




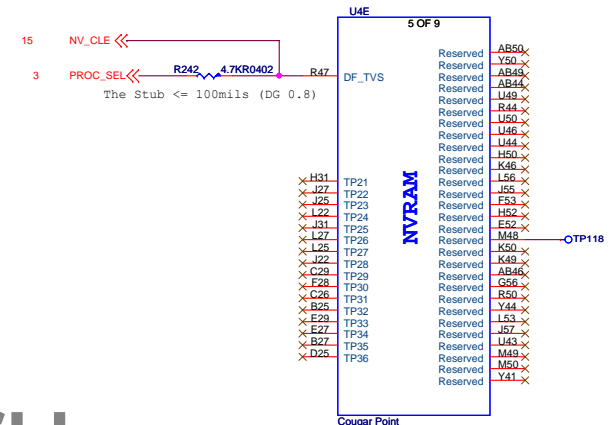
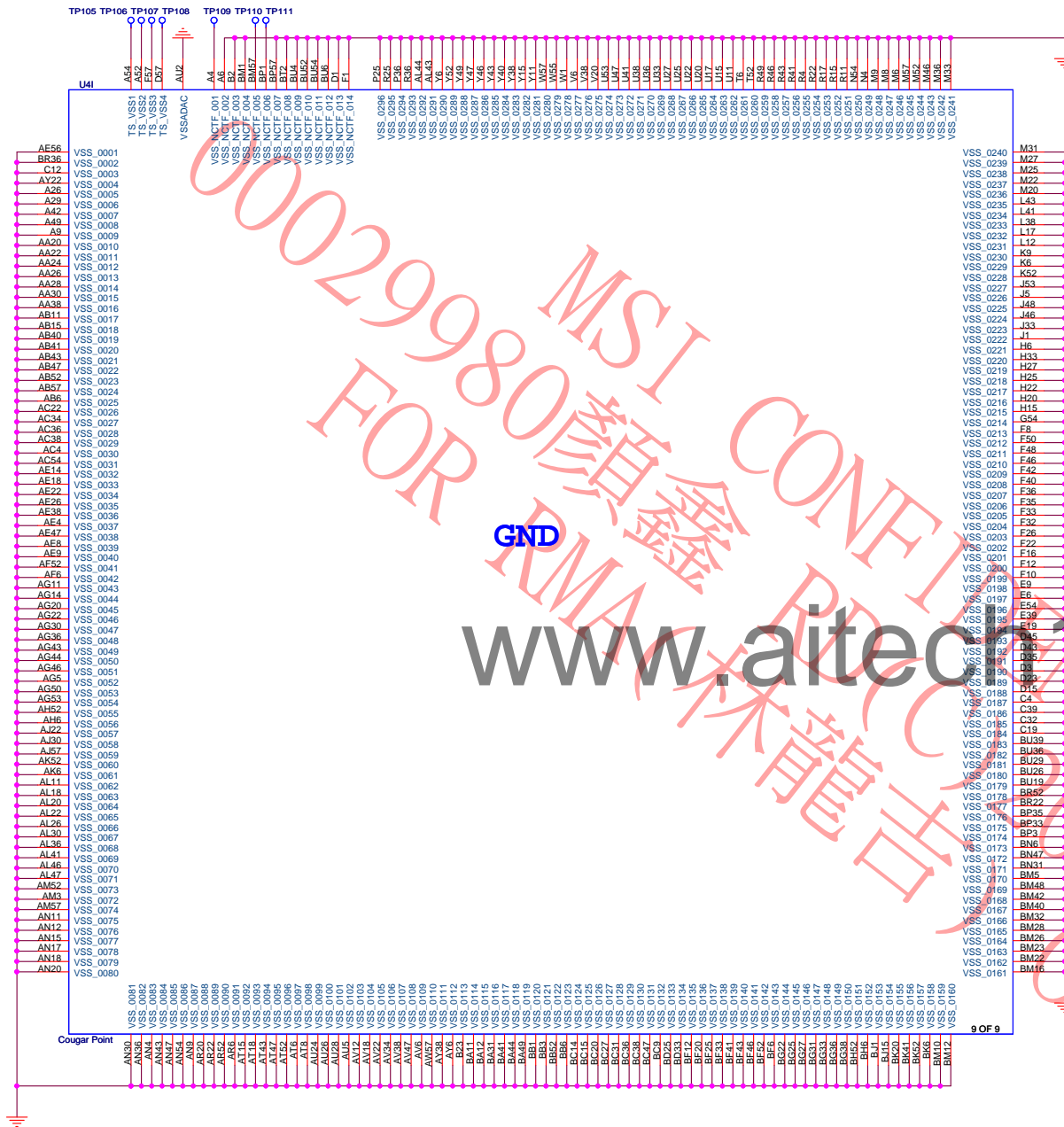




```
PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A
```



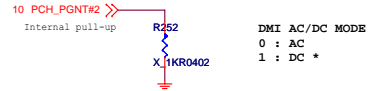
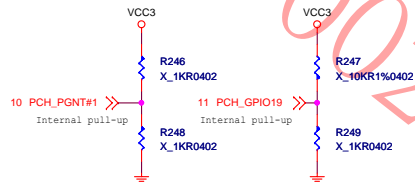




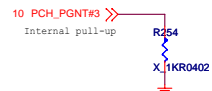


# PCH Straps

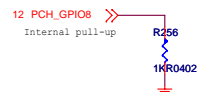
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



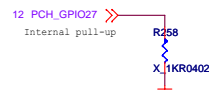
DMI AC/DC MODE  
0 : AC  
1 : DC \*



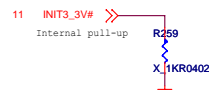
Topblock swap override when pull-low  
Signal has a weak internal pull-up



GPI08  
0 : Integrated Clocking Enable (FCIM)\*  
1 : Buffer Through Mode Enable (BTM)



GPI027  
0 : OD FLL VR disabled  
1 : OD FLL VR enabled \*  
Signal has a weak internal pull-up



INIT3\_3V#  
0 : INIT3\_3V to asserted for 16 PCI clock  
to reset the processor by some events occur  
1 : Can not to reset the processor



INTVRMEM  
0 : DISABLE INTERNAL VRM  
1 : ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the  
integrated GbE only operates at 10/100 Mbps during S3-S5.



DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V  
regulators. Must be connected even when not supporting DSW.

HDA\_SDO  
Disable ME in Manufacturing Mode  
when pull LOW ????



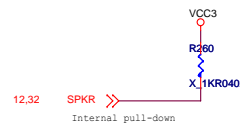
HDA\_SYNC  
OD FLL VR SUPPLY SEL  
0 : 1.8V SUPPLY \*  
1 : 1.5V SUPPLY



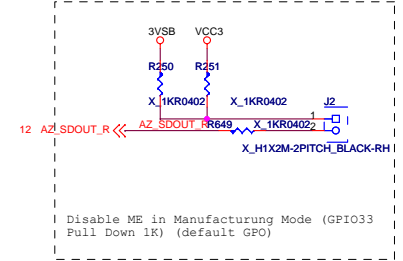
GPI015  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



Disable ME in Manufacturing Mode (GPI033  
Pull Down 1K) (default GPO)

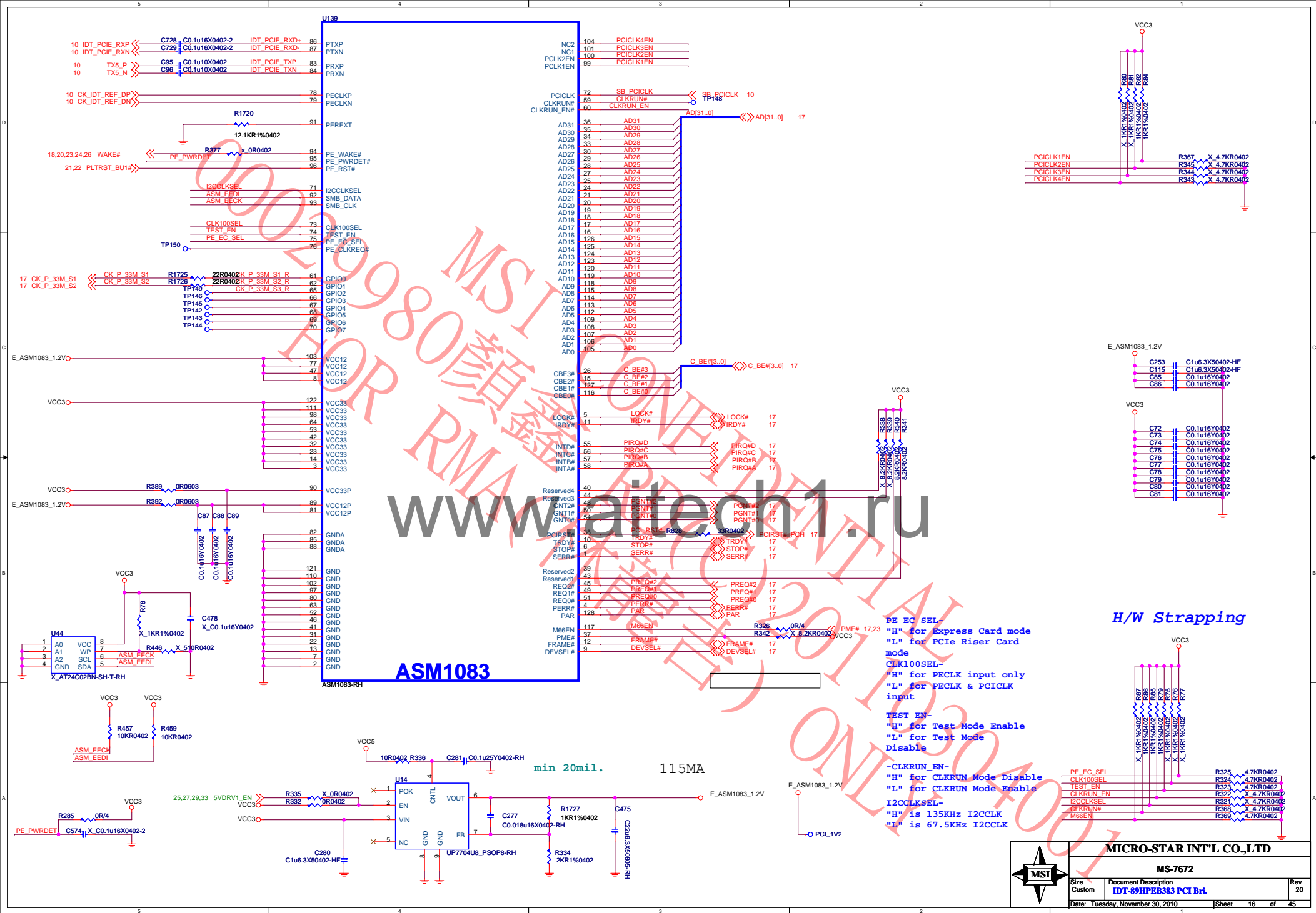


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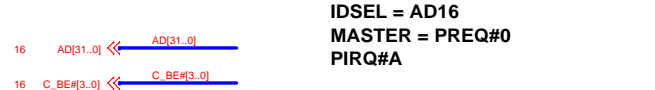
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-12V +12V



## VCC3



10/10



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Size  
Custom

Document Description  
PCI Slot 1 & 2 & 3

Date: T

Monday, November 30, 2010

Date: \_\_\_\_\_

Wednesday, November 30, 2010

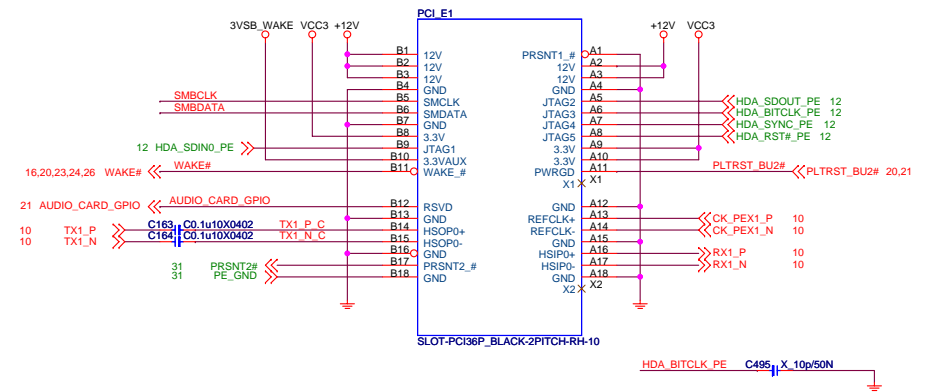
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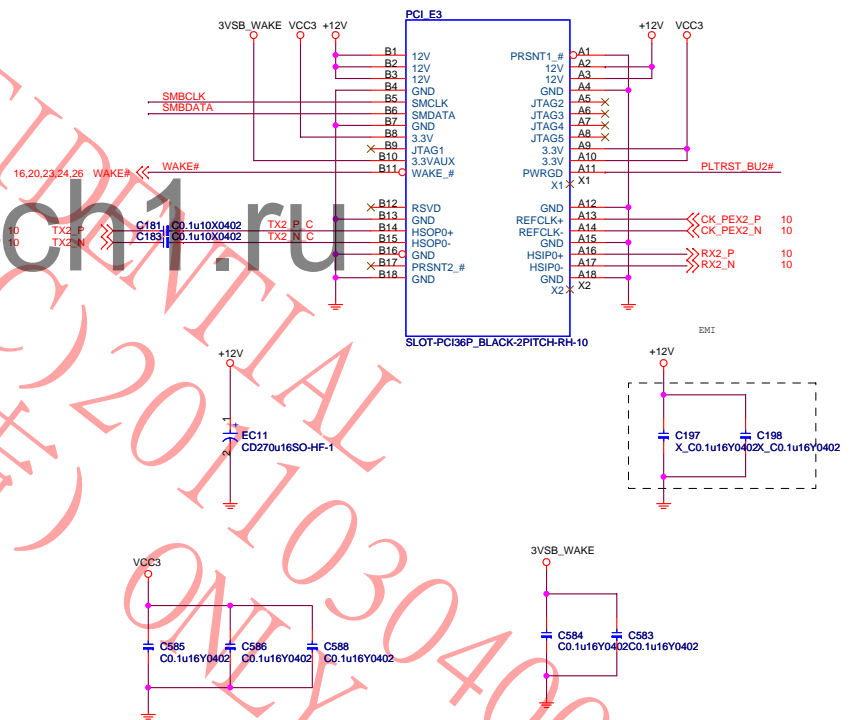
# PCI Express X16 slot

# HDA co-lay PCIex1

## PCI EXPRESS x1-PORT



## PCI EXPRESS x1-PORT



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Trace width > 200 mils

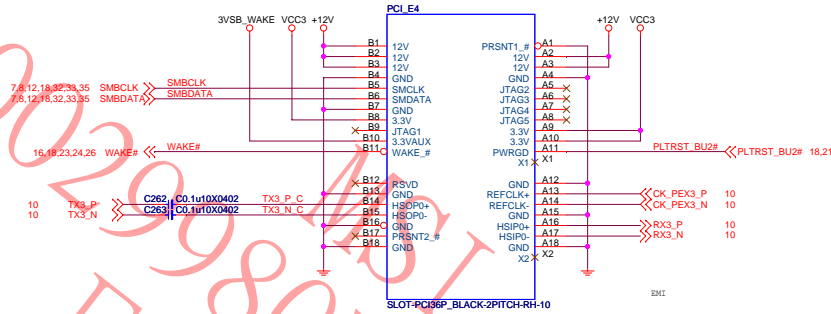


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# PCI EXPRESS x1-PORT

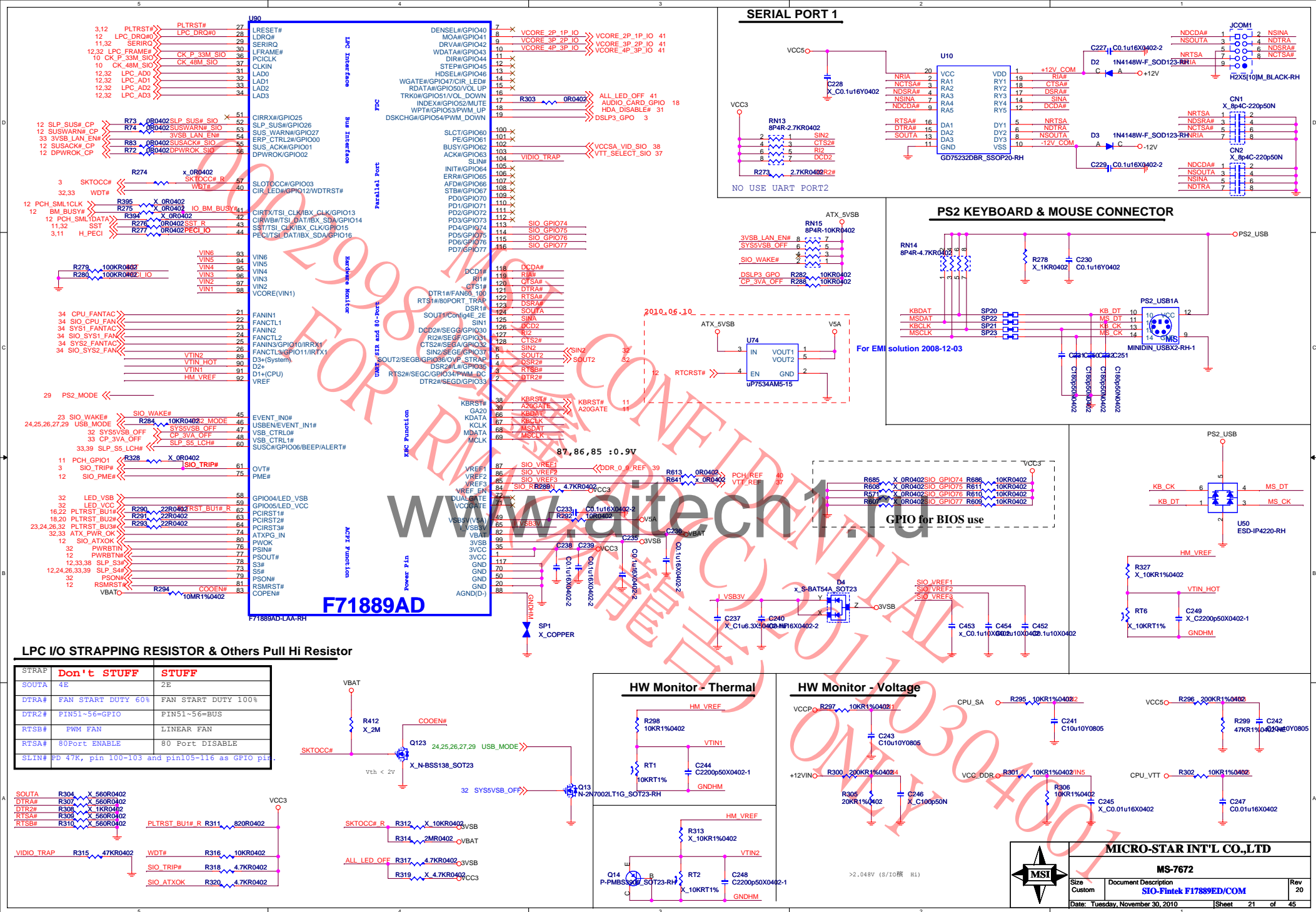


# PCI EXPRESS x1-PORT

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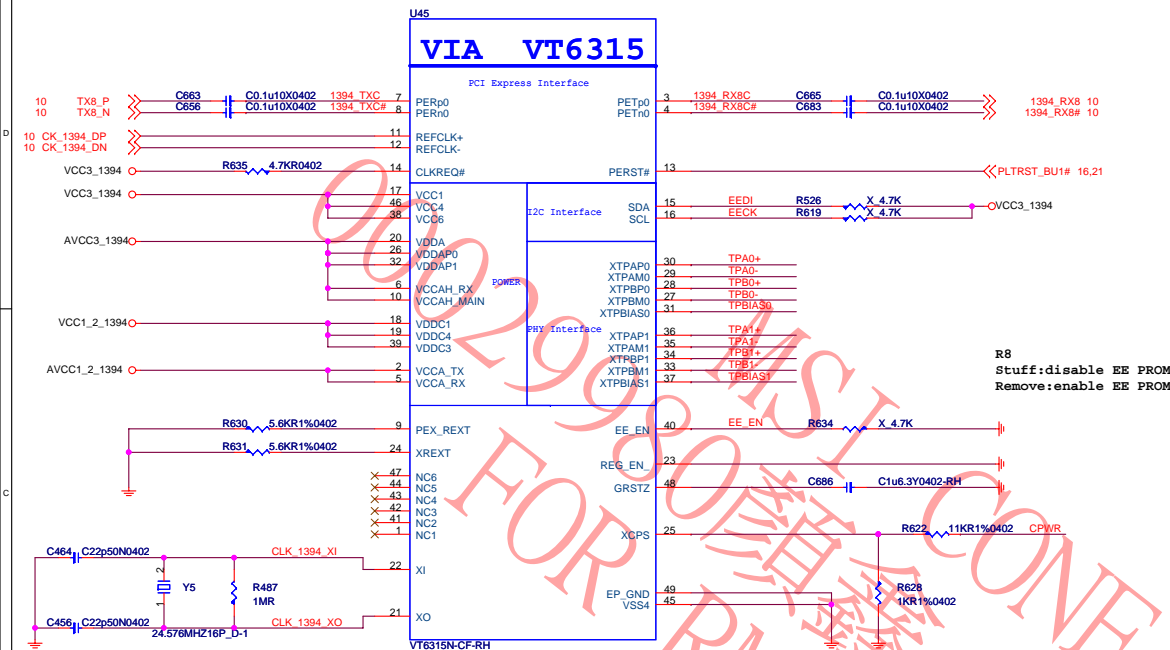
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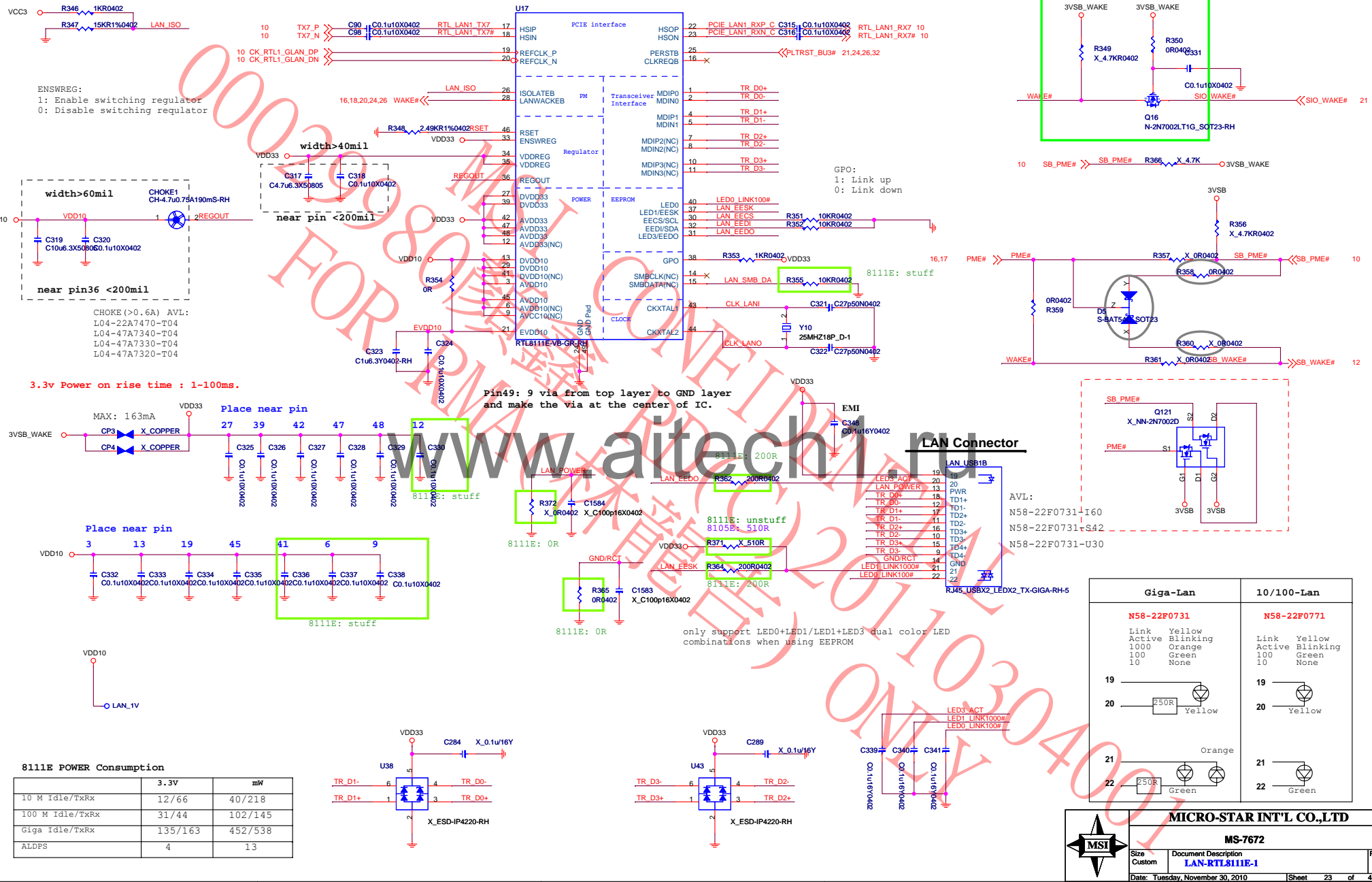


# 1394 CONTROLLER





### LAN/PCIE/PCI Wake Up CTRL Circuit



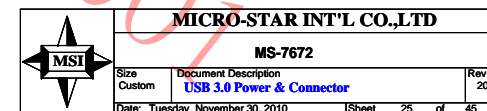
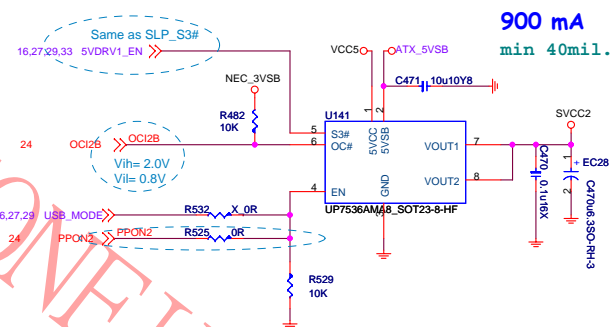
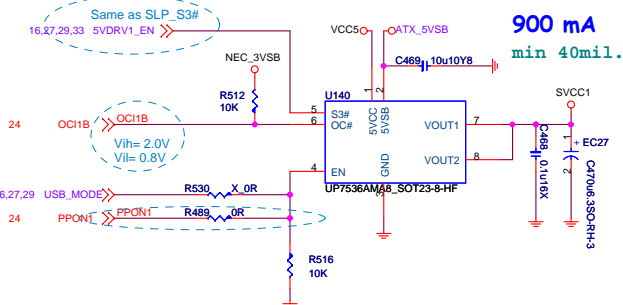
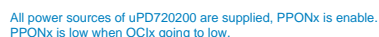
8111E POWER Consumption		
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

Giga-Lan	10/100-Lan																		
<p><b>N58-22F0731</b></p> <table> <tr> <td>Link</td> <td>Yellow</td> </tr> <tr> <td>Active</td> <td>Blinking</td> </tr> <tr> <td>1000</td> <td>Orange</td> </tr> <tr> <td>100</td> <td>Green</td> </tr> <tr> <td>10</td> <td>None</td> </tr> </table>	Link	Yellow	Active	Blinking	1000	Orange	100	Green	10	None	<p><b>N58-22F0771</b></p> <table> <tr> <td>Link</td> <td>Yellow</td> </tr> <tr> <td>Active</td> <td>Blinking</td> </tr> <tr> <td>100</td> <td>Green</td> </tr> <tr> <td>10</td> <td>None</td> </tr> </table>	Link	Yellow	Active	Blinking	100	Green	10	None
Link	Yellow																		
Active	Blinking																		
1000	Orange																		
100	Green																		
10	None																		
Link	Yellow																		
Active	Blinking																		
100	Green																		
10	None																		





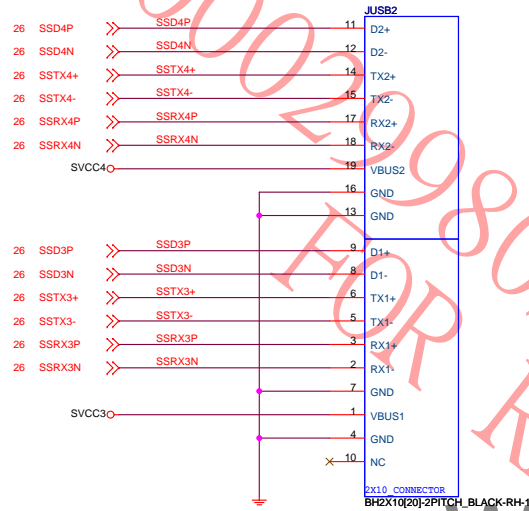




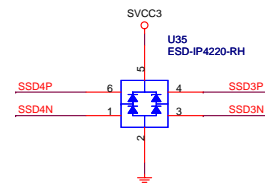
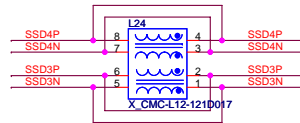
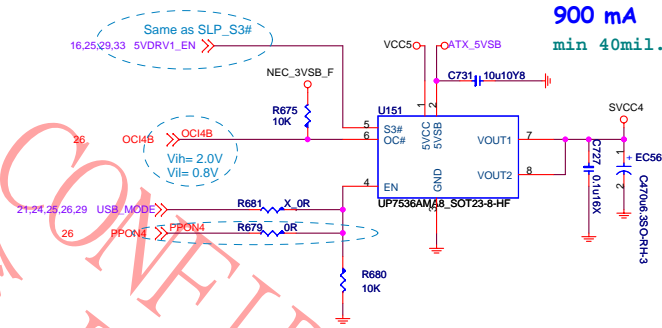
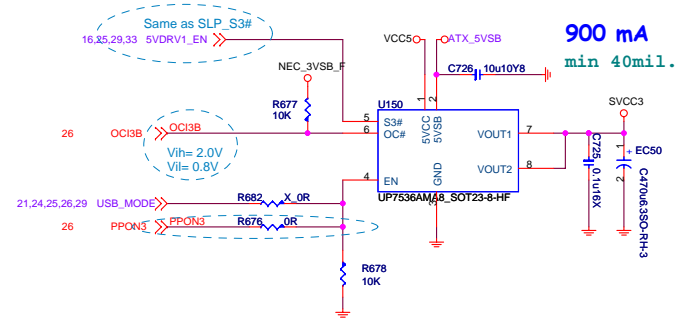








All power sources of uPD720200 are supplied, PPONx is enable.  
PPONx is low when OCix going to low.



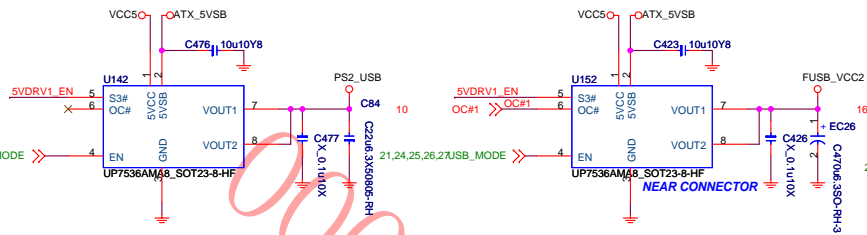
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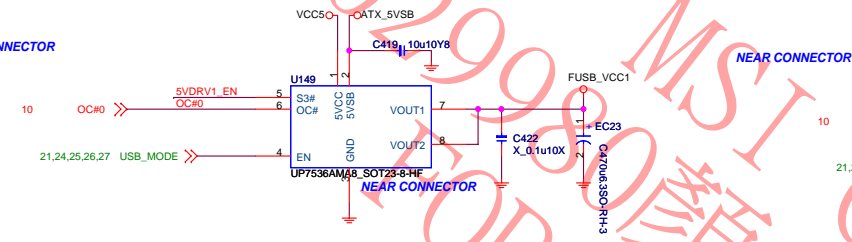


## Front USB Connector

### USB POWER FOR PORT 11,12

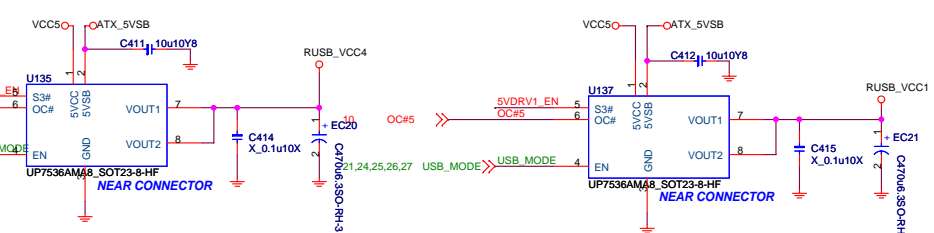


### USB POWER FOR PORT 11,12

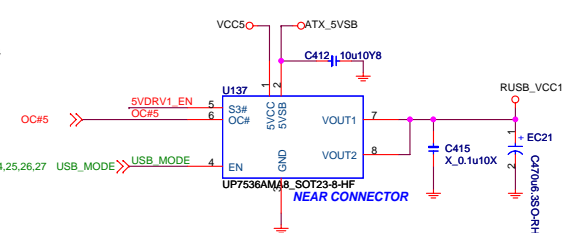


## Rear USB Connector

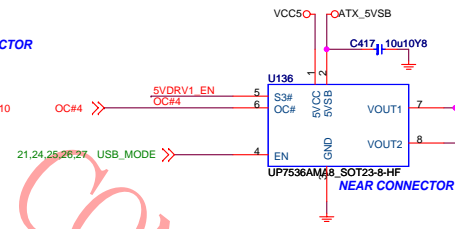
### USB POWER FOR PORT 4,5



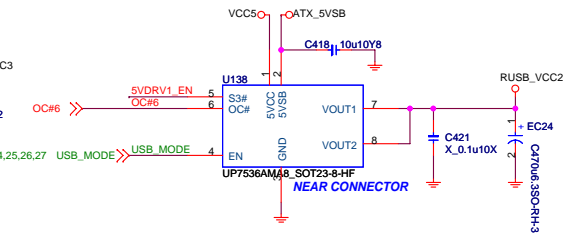
### USB POWER FOR PORT 6,7



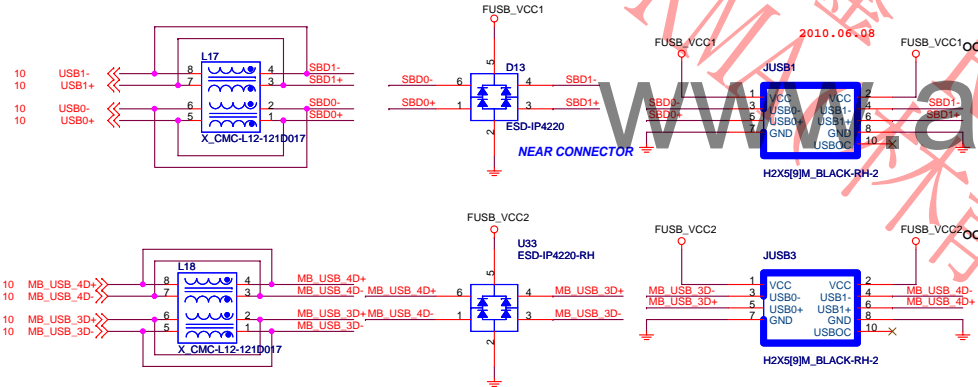
### USB POWER FOR PORT 11,12



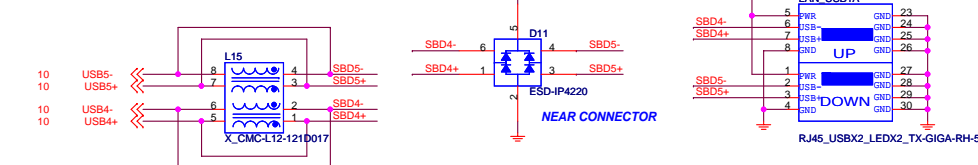
### USB POWER FOR PORT 8,9



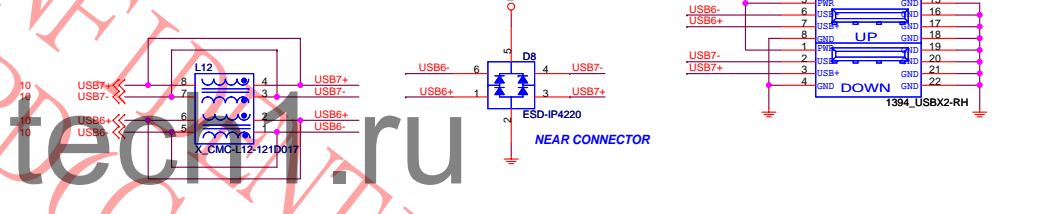
### FRONT USB PORT 4,5(With RJ45)



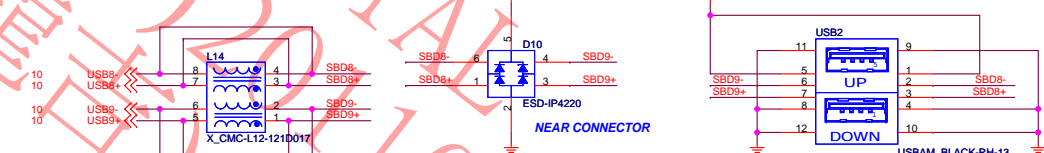
### FRONT USB PORT 4,5(With RJ45)



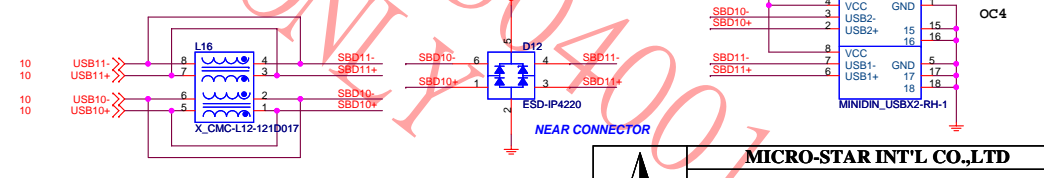
### REAR USB PORT 12,13 (With 1394&ESATA)



### REAR USB PORT 8,9 (With ESATA)



### REAR USB PORT 8,9 (With PS2)



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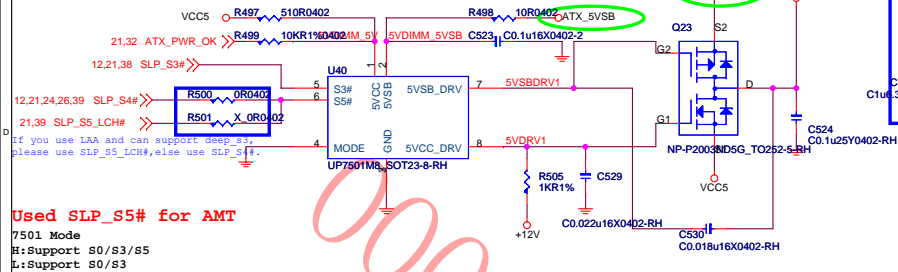




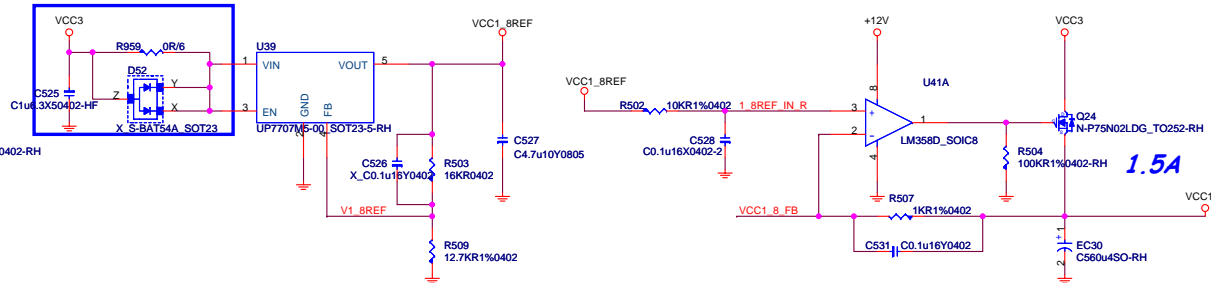




## 5VDIMM FOR DDR

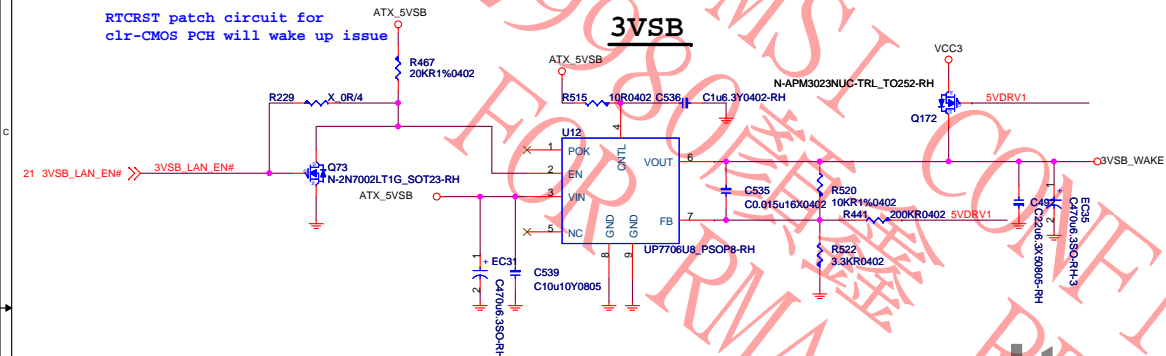


## VCC1\_8REF

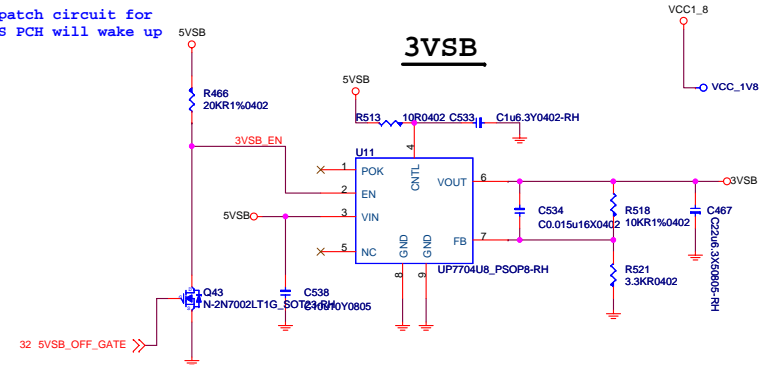


## 3VSB\_WAKE

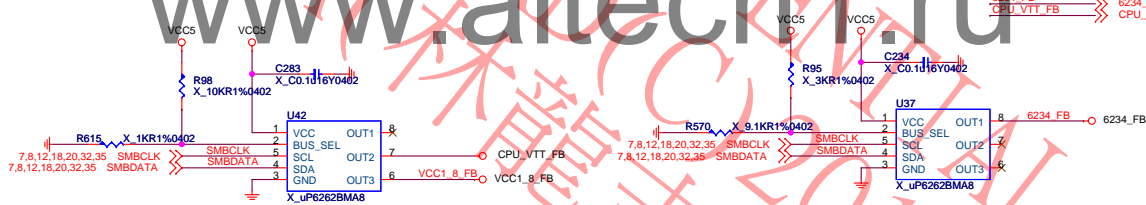
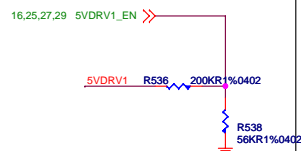
RTCST patch circuit for  
clr-CMOS PCH will wake up issue



RTCST patch circuit for  
clr-CMOS PCH will wake up  
issue



## USB MODE

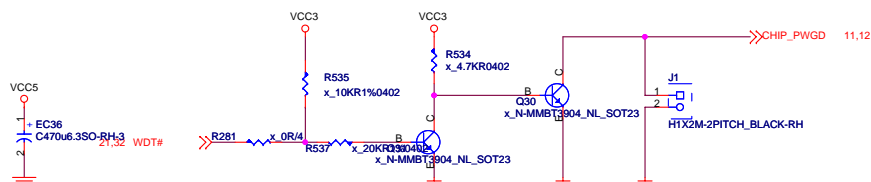


## UPI VOLTAGE CONSOLE

0x20 : RH=10K, RL=OPEN

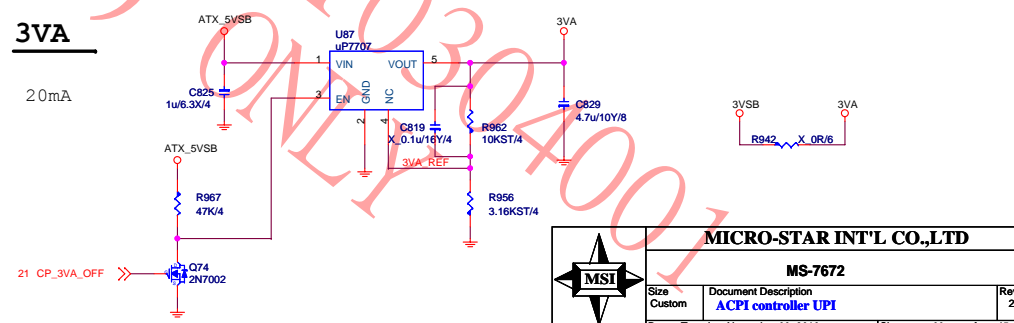
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

## WATCH DOG



## 3VA

20mA

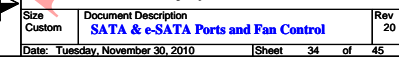
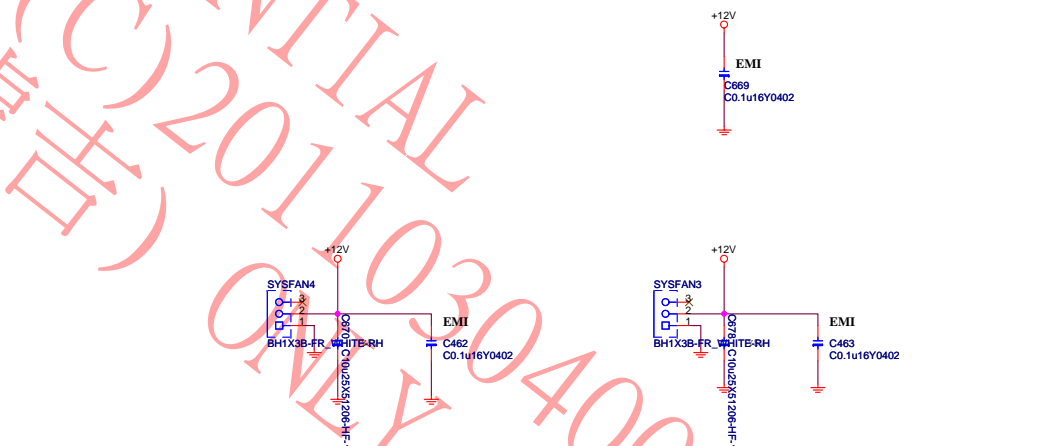
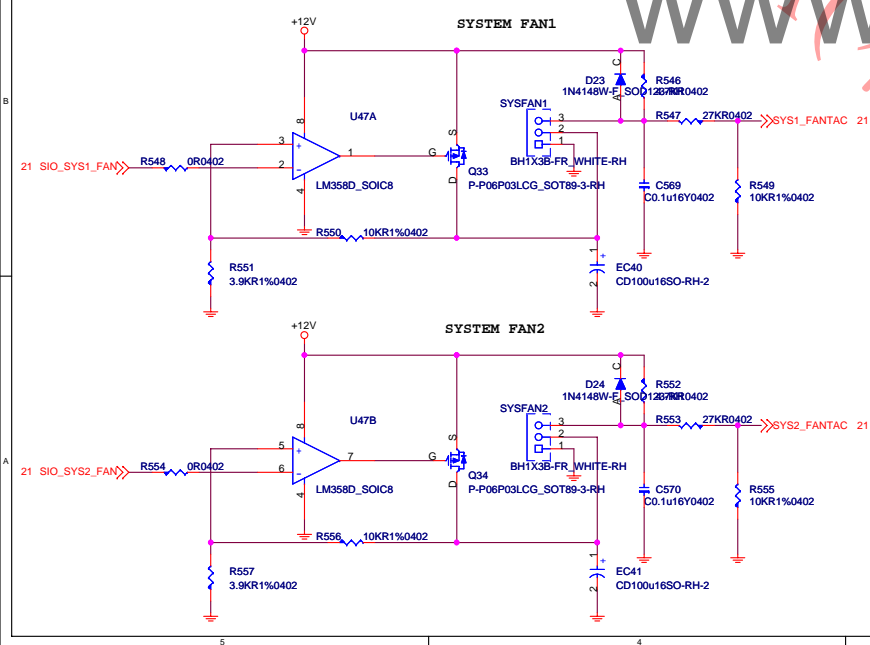
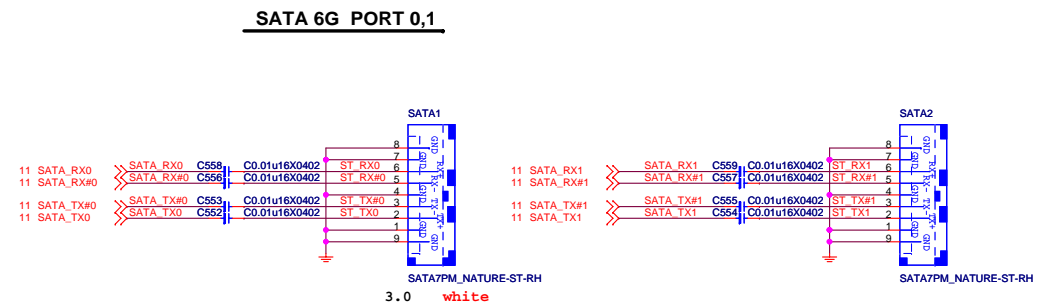


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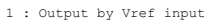
Size	Custom	Document Description	Rev
Doc	ACPI controller UPI		20
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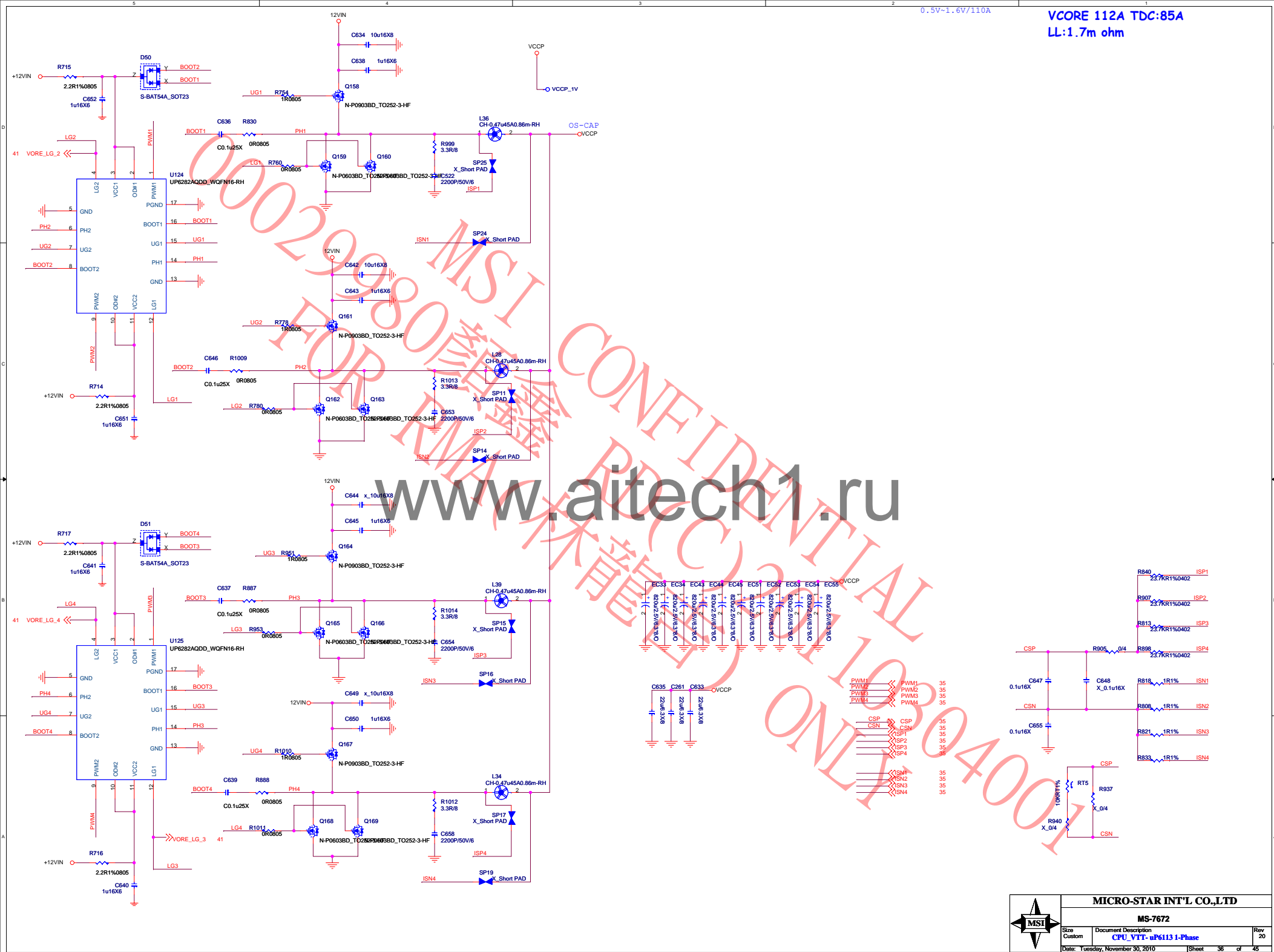
CPU\_VTT            3VSB



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Size Custom	Document Description <b>VRD12 - ISL6234 6+2Phase</b>	Rev 20
Date: Tuesday, November 30, 2010		Sheet 35 of 45



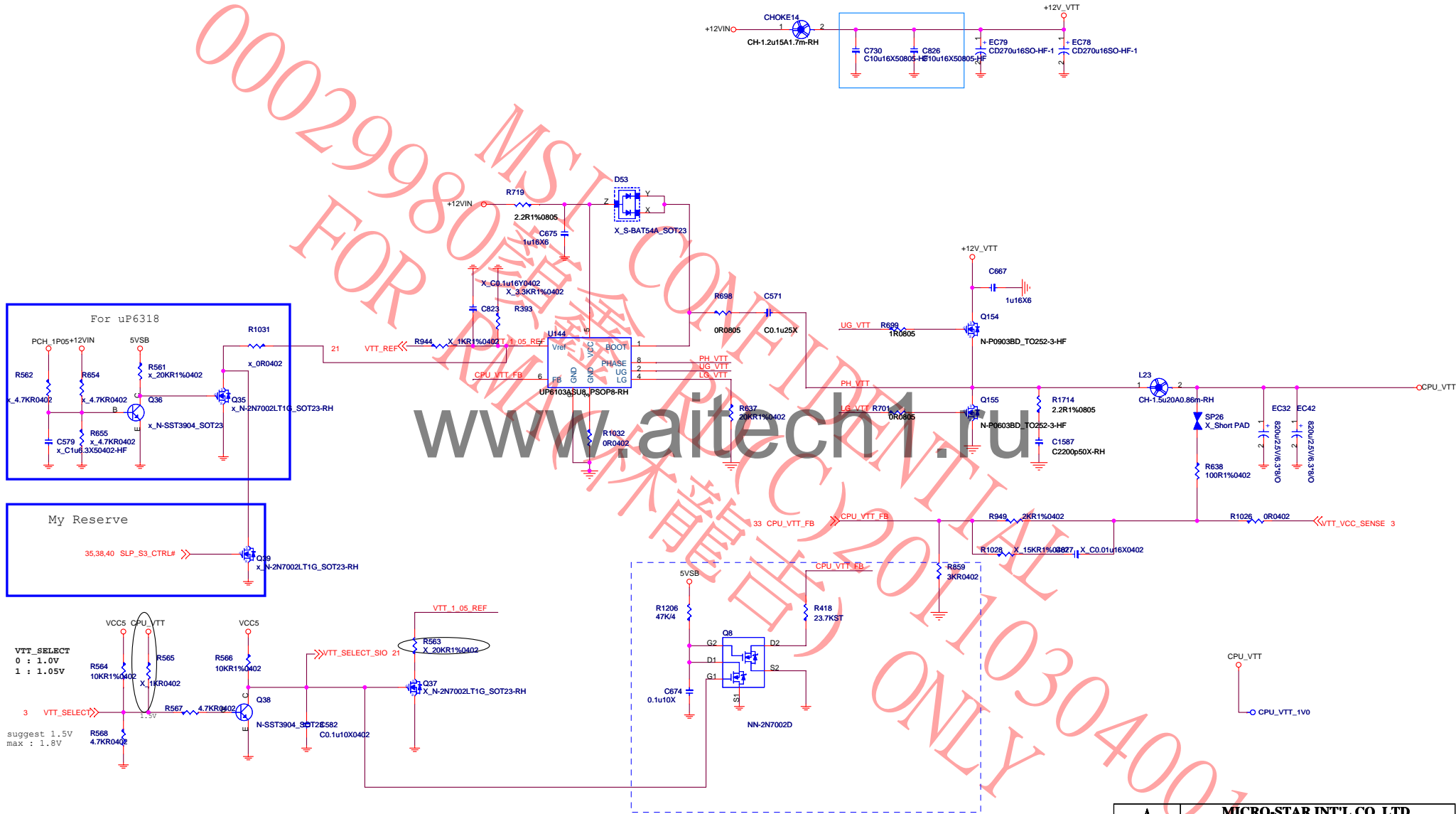




CPU\_VTT:1.05/1.00

CPU VTT 8.2A

$$I_{ripple} = 1.9(v_{tt}) + 1.8(sa)$$
$$5 \times 2 = 10A > 3.8A$$

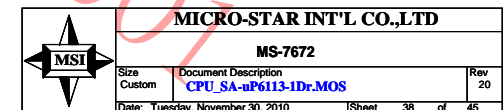
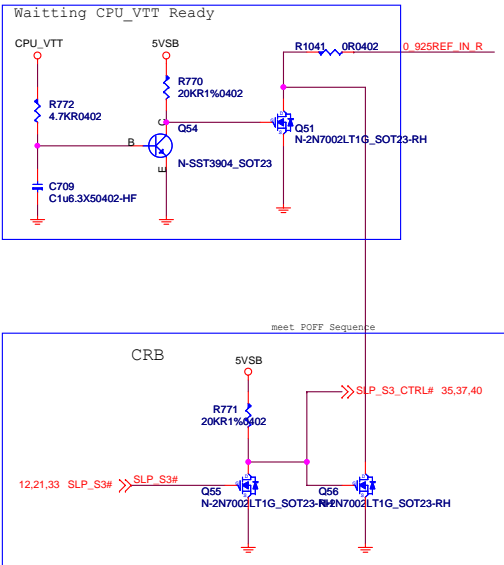


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Custom	CPU_VTT- uP6138 1-Phase	20
Date: Tuesday, November 30, 2010		Sheet 37 of 45



**SA Core = 8.8A**

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4.5A FOR CPU  
15A FOR 4DIMM  
1A FOR DDR VTT



## DDR VTT Power



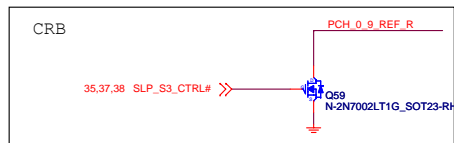
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Rev	20
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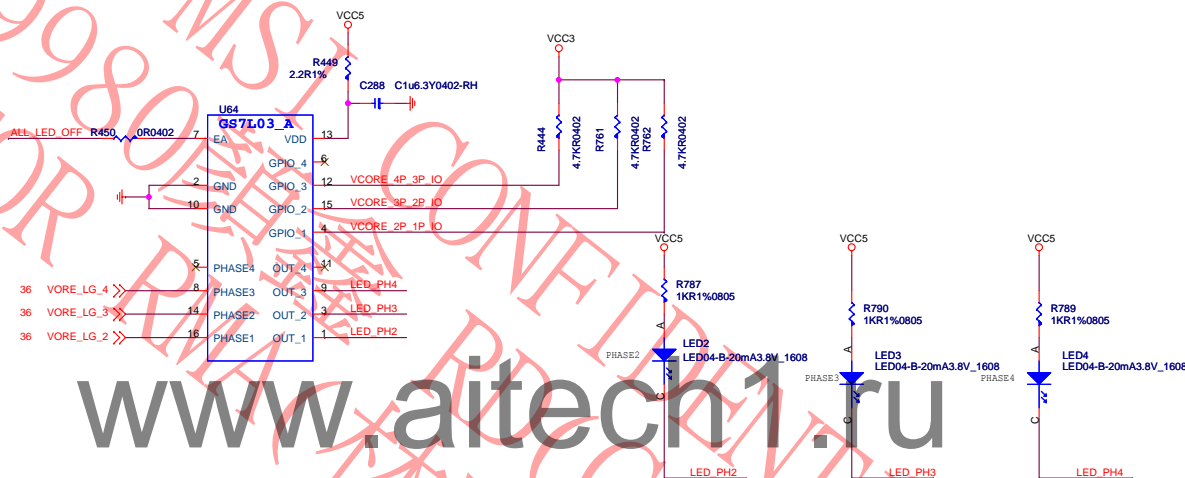
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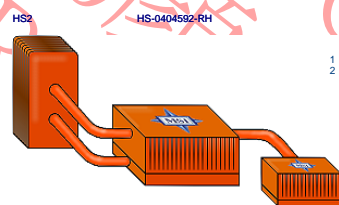
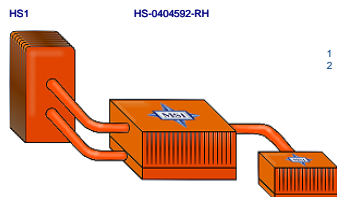
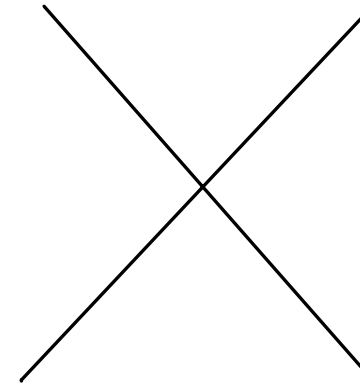


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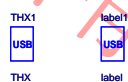
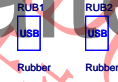
Size Custom	Document Description <b>PHASE Dropping &amp; LED</b>	Rev 20
Date: Tuesday, November 30, 2010		Sheet 41 of 45



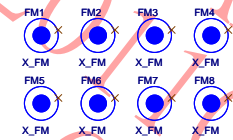


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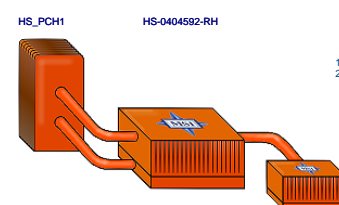
## Simulation



## Optical Fiducial Marks-120

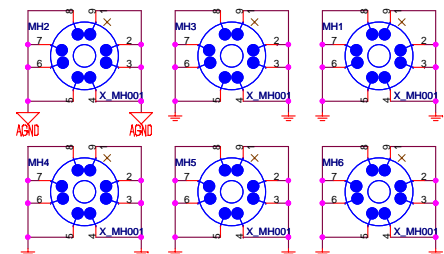


## Optical Fiducial Marks-100



7581\_11  
PD0-0758111-E48, 驢地, 27, 驢  
PD0-0758111-G37, 驢, 27, 驢  
吹邻紅 (MSIS)  
吹邻紅 (MSIS)

## Mounting Holes



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